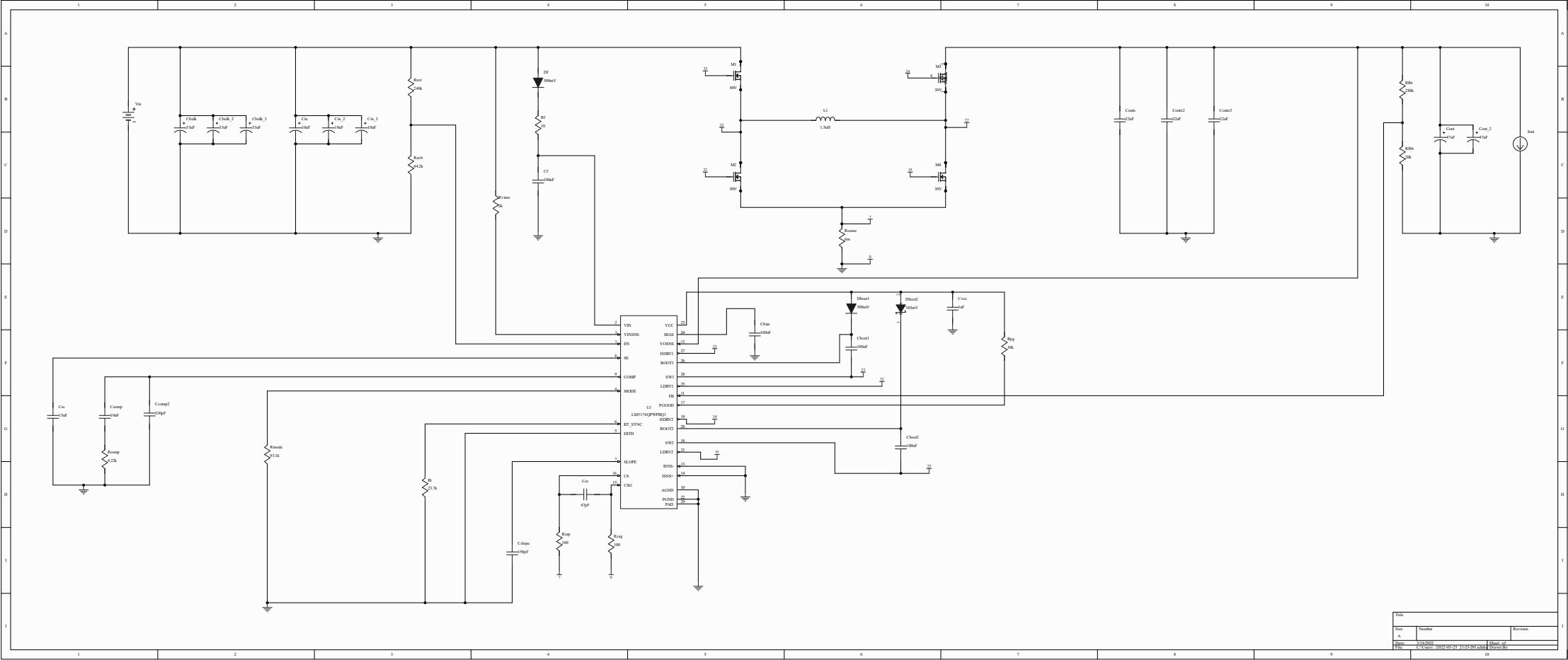


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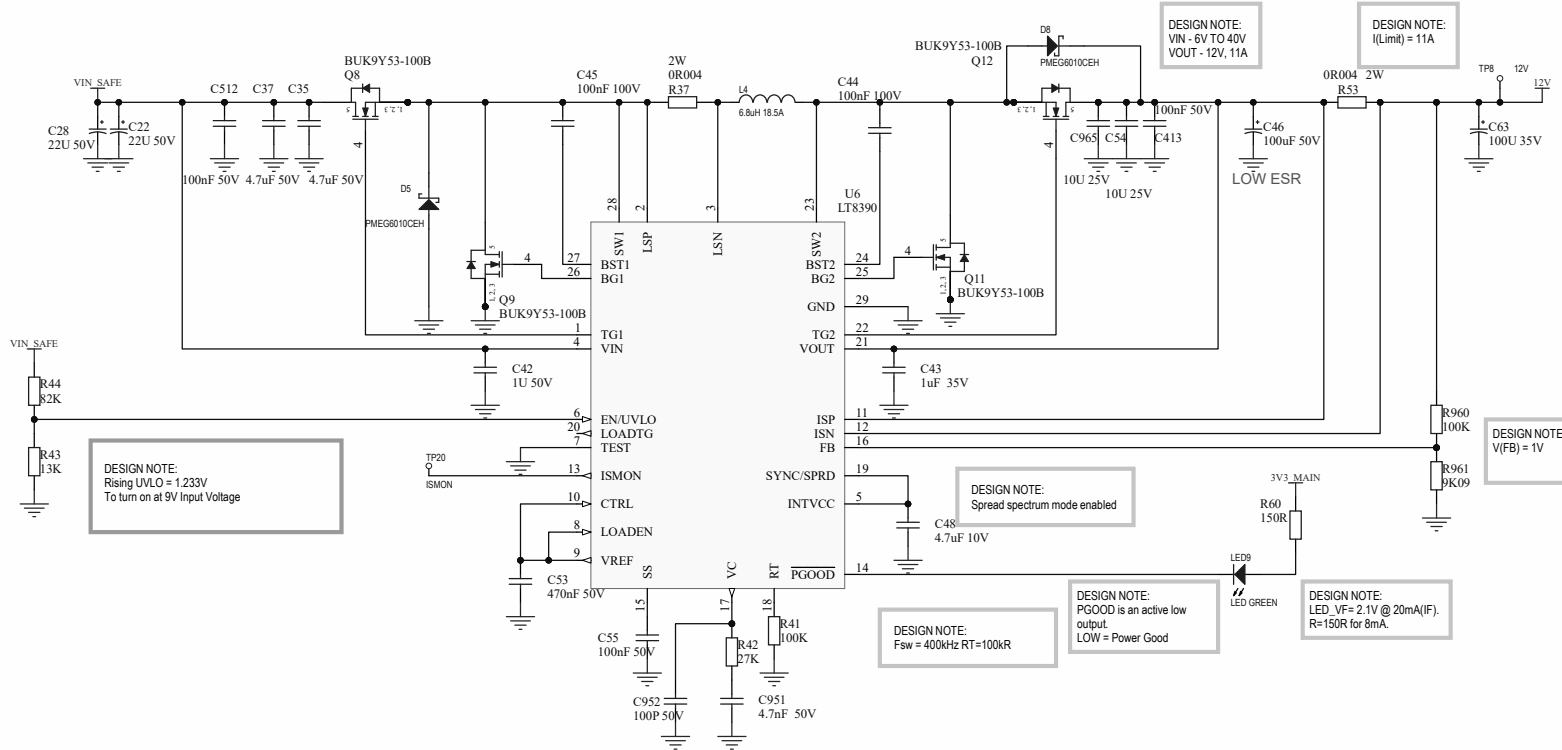
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12V PSU

DESIGN NOTE:
TURNS ON WITH VIN

DESIGN NOTE:
Total Load = 10A

Vin = 9-36V, Vout = 12V @ 11A



LAYOUT NOTE:

The basic PC board layout requires a dedicated ground plane layer. Also, for high current, a multilayer board provides heat sinking for power components.

-The ground plane layer should not have any traces and it should be as close as possible to the layer with power MOSFETs.

- Place CIN, switch A, switch B and DB in one compact area. Place COUT, switch C, switch D and DD in one compact area.

- Use immediate vias to connect the components to the ground plane.

- Use several large vias for each power component.

- Use planes for VIN and VOUT to maintain good voltage filtering and to keep power losses low.

- Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. Connect the copper areas to any DC net (VIN or GND).

- Separate the signal and power grounds. All small-signal components should return to the exposed GND pad

from the bottom, which is then tied to the power GND close to the sources of switch B and switch C.

- Place switch A and switch C as close to the controller as possible, keeping the PGND, BG and SW traces short.

- Keep the high dV/dT SW1, SW2, BST1, BST2, TG1 and TG2 nodes away from sensitive small-signal nodes.

- The path formed by switch A, switch B, DB and the CIN capacitor should have short leads and PCB trace lengths. The path formed by switch C, switch D, DD and the COUT capacitor also should have short leads and PCB trace lengths.

- The output capacitor (-) terminals should be connected as close as possible to the (-) terminals of the input capacitor.

- Connect the top driver boost capacitor CBST1 closely to the BST1 and SW1 pins. Connect the top driver boost capacitor CBST2 closely to the BST2 and SW2 pins.

- Connect the input capacitors CIN and output capacitors COUT closely to the power MOSFETs. These capacitors carry the MOSFET AC current.

- Route LSP and LSN traces together with minimum PCB trace spacing. Avoid sense lines pass through noisy areas, such as switch nodes. The filter capacitor between LSP and LSN should be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the RSENSE resistor. Low ESL sense resistor is recommended.

- Connect the VC pin compensation network close to the IC, between VC and the signal ground. The capacitor helps to filter the effects of PCB noise and output voltage ripple voltage from the compensation loop.

- Connect the INTVCC bypass capacitor, CINTVCC, close to the IC, between the INTVCC and the power ground. This capacitor carries the MOSFET drivers' current peaks. An additional 1uF ceramic capacitor placed immediately next to the INTVCC pin and power ground can help improve noise performance substantially.



Digital Technology Int
31 Affleck rd
Perth Airport WA 6105
Western Australia

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Checked:	PCB No:		
Approved:	Drawing No:	Drawing Revision:	Size: A3
Date Released:	File: 12V PSU - OLD LT.SchDoc		Sheet 4 of 20